## Remarks

Claims 1-8 are pending in the application. Claims 1-5, and 8 have been rejected under 35 U.S.C. § 102(b), and claim 1 has been rejected under 35 U.S.C. § 102(e). Additionally, claims 6 and 7 have been rejected under 35 U.S.C. § 103(a). In view of the following remarks, reconsideration and withdrawal of these grounds of rejection is requested.

## Claim Objections

The Examiner objects to claims 3 and 4 as claiming the same invention. Applicant submits that claims 3 and 4 claim different inventions. Claim 3 is directed to a "phase modulator" and claim 4 is directed to only a "modulator" (emphasis added). As is well known to those of ordinary skill in the art, various modulators and modulation schemes exist outside of phase modulation. For example, amplitude modulation (AM), frequency modulation (FM), and other modulation schemes exist. The specification of the present application makes note of this fact at Paragraph [0019]: "those of ordinary skill in the art will realize that other methods of modulation are equally as applicable..." Accordingly, reconsideration and withdrawal of this objection is respectfully requested.

## Claim Rejections Under 35 U.S.C. § 102

Claims 1 and 5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Holden et al. (U.S. Pat. No. 6,411,655). For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

The present invention comprises, in one exemplary embodiment, a signal transmission apparatus 100 including a base band signal generation and coding ("BBSGC") portion 110, a rectangular to polar converter 120, a phase modulator 130, a variable gain amplifier 140, and a digital amplitude restoration circuit 200.

In operation, the BBSGC portion 110 converts an input analog wave I into digital format and provides any necessary coding (see, specification, Paragraph [0016]). The digitized (and possibly coded) wave is then converted into polar format by the rectangular to polar converter 120, resulting in amplitude (m) and phase ($\phi$) components (see, specification, Paragraph [0017]). The amplitude portion (m) is then provided to the digital amplitude restoration circuit 200 which includes an amplitude mapping circuit 210. The amplitude mapping circuit 210 converts the amplitude portion (m) into a binary value (e.g., with bits $b_1 - b_n$). The binary value (or digital word "DW" as it is also referred to in the specification) is applied to a series of power amplifiers through a digital gain control circuit 220 to control the gain level of the power amplifiers (see, specification, Paragraph [0021]).

Independent claim 1 recites:

> An apparatus comprising: an amplitude mapping circuit <u>for converting at least a portion of an amplitude signal to a binary value</u>; and, a plurality of amplifiers coupled to the amplitude mapping circuit, wherein <u>the binary value</u> is transmitted to at least one of the plurality of amplifiers to specify a gain level of the amplifier. [emphasis added].

Thus, claim 1 requires an "amplitude mapping circuit" which converts at least a portion of an "amplitude signal" into a "binary value." Claim 1 also requires that such "binary value" be transmitted to at least one of a plurality of amplifiers to specify a "gain level." Holden fails to

disclose, teach or suggest such an invention.

Holden teaches a system which includes a digital signal processor 10 which supplies a sequence of phase values ($\phi$) and amplitude control bits ($b_1$-$b_n$) (See Fig. 1). However, claim 1 requires an amplitude mapping circuit "for converting at least a portion of an amplitude signal to a binary value." Holden does not disclose, teach or suggest "converting" an amplitude signal into a binary value. In fact, the digital signal processor 10 of Holden does not 'convert' anything (because it has no inputs, only outputs), it merely generates a series of amplitude control bits ($b_1$-$b_n$). Accordingly, because Holden does not disclose, teach or suggest a circuit which converts an "amplitude signal" into a "binary value," reconsideration and withdrawal of this ground of rejection with respect to independent claim 1, and claims 3 and 5 dependent thereon, is respectfully requested.

Claims 1-5 and 8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Grondahl (U.S. Pat. No. 5,936,464). For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

As noted above, independent claim 1 requires an "amplitude mapping circuit" which converts at least a portion of an "amplitude signal" into a "binary value," where the "binary value" be transmitted to at least one of a plurality of amplifiers to specify a "gain level." Grondahl fails to disclose, teach or suggest such an invention.

Grondahl teaches an Envelope Elimination and Restoration (EER) amplifier 10 which divides a signal to be amplified into amplitude and phase paths (See Fig. 1). The amplitude path includes an envelope detector 220 and an envelope amplifier 270. The phase path includes a

time delay element 230, limiter 240, driver amplifier 250, and power amplifier 260. The driver amplifier 250 includes a variable amplifier 252 which is driven by the output of an analog to digital (A/D) converter 257.

Grondahl fails to disclose, teach or suggest a "plurality of amplifiers coupled to [an] amplitude mapping circuit" to each receive a binary value specifying a "gain level." Grondahl teaches only one amplifier (variable amplifier 252) coupled to the A/D converter 257 (which the Examiner contends corresponds to the "amplitude mapping circuit" limitation of claim 1). The amplifier 253 of Grondahl is not coupled to the A/D converter 257, and thus Grondahl fails to disclose or suggest a "plurality of amplifiers" coupled to an "amplitude mapping circuit," as specified in claim 1. Hence, reconsideration and withdrawal of this ground of rejection with respect to claim 1, and claims 2-7 dependent thereon, is respectfully requested.

Independent claim 8 includes similar limitations to those discussed above with reference to independent claim 1, in particular the limitation of a binary value generated from a amplitude signal which is supplied to a "plurality of amplifiers." For example, claim 8 recites:

> A method for processing a signal, comprising the steps of: separating the signal into amplitude and phase components; generating a binary representation of at least a portion of the amplitude component; and, specifying a gain level of one of a plurality of amplifiers in response to the generated binary representation. [emphasis added].

Thus, claim 8 requires a method wherein a gain level of one of a "plurality of amplifiers". As discussed above with reference to claim 1, Grondahl fails to disclose, teach or suggest a "plurality of amplifiers" which have their gain levels specified by a binary signal. Therefore, for at least those reasons discussed above with respect to claim 1, reconsideration and withdrawal of

this rejection with respect to claim 8 is respectfully requested.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Husseini (U.S. Pat. No. 6,859,098). For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

As noted above, independent claim 1 requires an "amplitude mapping circuit" which converts at least a portion of an "amplitude signal" into a "binary value," where the "binary value" be transmitted to at least one of a plurality of amplifiers to specify a "gain level." Husseini fails to disclose, teach or suggest such an invention.

Husseini teaches a system 200 "for processing of electromagnetic waves and signals" including a control port 203 for receiving an "amplitude component" ($A_m$) and a control port 206 for receiving a "phase component" ($P_m$) (See Fig. 1; col. 3, lines 24-40). In one exemplary embodiment, a scaling component 609 receives "a control signal $V_{amp}$ from [a] controller 610 to adjust the peak-to-peak level of the envelope of the amplitude component [(i.e., $A_m$)]..." (see, col. 7, lines 35-45). Husseini specifically notes that "scaling may be accomplished in baseband," meaning in the analog domain (see col. 7, lines 30-37). The output of the scaling component 609 is thus an <u>analog</u>, not a digital, value (emphasis added). Thus, the scaling component 609 cannot meet the "amplitude mapping circuit" limitation of claim 1 because it does not produce a "binary value" at its output. Accordingly, reconsideration and withdrawal of this ground of rejection with respect to claim 1 is respectfully requested.

## Claim Rejections Under 35 U.S.C. § 103

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being obvious over Holden, Grondahl or Husseini in view of Choi (U.S. Pat. No. 6,765,439). For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

As discussed in detail above, all of Holden, Grondahl and Husseini fail to disclose, teach or suggest a circuit which converts an "amplitude signal" into a "binary value" which is supplied to a "plurality of amplifiers" to specify a "gain level," as recited in independent claim 1 upon which claims 6 and 7 depend. Hence, for at least those reasons highlighted above with reference to claim 1, reconsideration and withdrawal of this ground of rejection with respect to claims 6 and 7 is respectfully requested.

## Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,

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